Listing of the Claims:

Claim 1 (Currently amended): A method for etching deep trenches in a substrate, comprising the steps of:

securing a wafer to an electrode in a plasma chamber, the wafer comprising a silicon substrate;

heating the wafer to a temperature of greater than 200 degrees Celsius; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer, wherein the deep trenches have a depth of greater than 8um, and wherein the deep trench etching is performed for a ground rule design ~~and a diameter~~ of 175nm or less.

Claim 2 (Original): The method as recited in claim 1, wherein the step of heating the wafer includes the step of heating the wafer to a temperature of between about 200 and about 450 degrees Celsius.

Claim 3 (Original): The method as recited in claim 1, wherein the step of heating the wafer includes the step of heating the electrode such that heat is transferred to the wafer to provide the temperature of greater than 200 degrees Celsius.

Claim 4 (Canceled).

Claim 5 (Original): The method as recited in claim 1, wherein the wafer is secured by clamping and wherein the step of securing the wafer includes the step of applying a backside pressure to the clamped wafer to achieve thermal contact between the wafer and the electrode.

Claim 6 (Original): The method as recited in claim 1, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to a reactive plasma including at least one of Cl_2, HBr, HCl and BCl_3.

Claim 7 (Original): The method as recited in claim 6, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to Ar.

Claim 8 (Original): The method as recited in claim 1, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to additive gases to increase selectivity between an etch mask and the substrate during formation of the trenches.

Claim 9 (Original): The method as recited in claim 8, wherein the additive gases include at least one of O_2 and N_2.

Claim 10 (Original): The method as recited in claim 8, wherein the additive gases include O_2 with a flow of between about 6 % to about 40 % of a total gas flow.

Claim 11 (Original): The method as recited in claim 8, wherein the additive gases include N_2 with a flow of between about 10 % to about 30 % of a total gas flow.

14 Claim 12 (Previously presented): A method for etching deep trenches in a substrate, comprising the steps of:

securing a wafer to an electrode in a plasma chamber, the wafer comprising a silicon substrate;

heating the wafer to a temperature of greater than 200 degrees Celsius; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of

the wafer, wherein the deep trenches have a depth of greater than 8um, and wherein the step of exposing the wafer to the reactive plasma includes the step exposing the wafer to a gas combination including Cl_2, BCl_3, Ar, O_2, and N_2.

11 Claim 13 (Original): The method as recited in claim 1, wherein the step of securing a wafer to an electrode includes securing the wafer in an unclamped state and the step of heating the wafer includes bombarding the wafer with plasma ions to generate heat.

15 Claim 14 (Currently amended): A method for etching deep trenches in a substrate, comprising the steps of;

forming a hardmask on a silicon substrate of a wafer;

patterning the hardmask;

securing the wafer to an electrode in a plasma chamber;

maintaining the electrode at a temperature of between about 200 and about 450 degrees Celsius to achieve about the same temperature in the wafer; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer in accordance with the hardmask pattern, wherein the deep trenches have a depth of

greater than 8um, and wherein the deep trench etching is performed for a ground rule design ~~and a diameter~~ of 175nm or less.

16 Claim 15 (Original): The method as recited in claim 14, wherein the wafer is secured by clamping and wherein the step of securing the wafer includes the step of applying a backside pressure to the clamped wafer to achieve thermal contact between the wafer and the electrode.

17 Claim 16 (Original): The method as recited in claim 14, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to a reactive plasma including at least one of Cl_2, HBr, HCl and BCl_3.

18 Claim 17 (Original): The method as recited in claim 16, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to Ar.

19 Claim 18 (Original): The method as recited in claim 16, wherein the step of exposing the wafer to the reactive plasma includes the step of exposing the wafer to additive gases to increase selectivity between an etch mask and the substrate during formation of the trenches.

20 Claim 19 (Original): The method as recited in claim 18, wherein the additive gases include at least one of O_2 and N_2.

21 Claim 20 (Original): The method as recited in claim 18, wherein the additive gases include O_2 with a flow of between about 6 % to about 40 % of a total gas flow.

22 Claim 21 (Original): The method as recited in claim 18, wherein the additive gases include N_2 with a flow of between about 10 % to about 30 % of a total gas flow.

25 Claim 22 (Previously presented): A method for etching deep trenches in a substrate, comprising the steps of;

forming a hardmask on a silicon substrate of a wafer;

patterning the hardmask;

securing the wafer to an electrode in a plasma chamber;

maintaining the electrode at a temperature of between about 200 and about 450 degrees Celsius to achieve about the same temperature in the wafer; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer in accordance with the hardmask pattern, wherein the deep trenches have a depth of greater than 8um, and wherein the step of exposing the wafer to the reactive plasma includes the step exposing the wafer to a gas combination including Cl_2, BCl_3, Ar, O_2, and N_2.

26 Claim 23 (Currently amended): A method for etching deep trenches in a substrate, comprising the steps of:

clamping a wafer onto a electrode in a plasma chamber, the wafer comprising a silicon substrate;

maintaining the electrode at an elevated temperature between of about 200 degrees and 450 degrees Celsius;

exposing the wafer to a reactive plasma including Cl_2, BCL_3, Ar, O_2, and N_2;

applying a backside pressure to the clamped wafer using He to achieve thermal contact between the wafer and the electrode such that the wafer is maintained at about the same temperature as the electrode; and

applying a bias power to the wafer electrode to accelerate ions from the plasma to achieve etching of the silicon substrate to form deep trenches, wherein the deep trenches have a depth of greater than 8um and wherein the deep trench etching is performed for a ground rule design of 175nm or less.

Claim 24 (Original): The method as recited in claim 23, wherein the O_2 includes a flow of between about 6 % to about 40 % of a total gas flow.

Claim 25 (Original): The method as recited in claim 23, wherein the N_2 includes a flow of between about 10 % to about 30 % of a total gas flow.

Claim 26 (Previously presented): The method as recited in claim 1, wherein the step of securing the wafer includes the step of applying a backside pressure of about 6 torr or greater to the secured wafer while maintaining a wafer temperature of about 200 degrees Celsius or greater.

Claim 27 (Previously presented): The method as recited in claim 1, wherein the step of heating the wafer includes the step of heating the wafer to a temperature of between about 300 and about 450 degrees Celsius.

27 Claim 28 (Previously presented): The method as recited in claim 14, wherein the step of securing the wafer includes the step of applying a backside pressure of about 6 torr or greater to the secured wafer while maintaining a wafer temperature of about 200 degrees Celsius or greater.

24 Claim 29 (Previously presented): The method as recited in claim 14, wherein the step of heating the wafer includes the step of heating the wafer to a temperature of between about 300 and about 450 degrees Celsius.

29 Claim 30 (Previously presented): The method as recited in claim 23, wherein the step of securing the wafer includes the step of applying a backside pressure of about 6 torr or greater to the secured wafer while maintaining a wafer temperature of about 200 degrees Celsius or greater.

30 Claim 31 (Previously presented): The method as recited in claim 23, wherein the step of heating the wafer includes the step of heating the wafer to a temperature of between about 300 and about 450 degrees Celsius.